REMARKS

The Examiner is thanked for reviewing the subject application. All claims are now believed to be in condition for Allowance, and Allowance is so requested.

The Examiner's FINAL restriction requirement is acknowledged. Non-elected claims 90-99 have been cancelled. A Divisional application will be filed at a later date. Method claims 26-28, which were mistakenly included in this Divisional application, have also been cancelled.

Reconsideration of the rejection of Claims 29-32, 38-48, and 80-89 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, is requested, based on the following.

Claims 29, 88 and 89 have been amended to clarify that the semiconductor substrate has semiconductor devices "formed thereon", as shown in Fig. 1. Semiconductor substrate 1 is shown in Fig. 1, and at page 9, lines 11-12, it is indicated that "silicon substrate 1 has transistors and other devices". It is of course well known that transistors and other devices are formed in and on semiconductor substrates as part of the process of manufacturing integrated circuits.

Also, Claims 29, 88 and 89 have been amended to clarify that the interconnecting metallization structure is "formed over and connected to" the devices. It is also of course well known that devices formed on a semiconductor substrate are connected together by metal lines formed above the devices, with the metal contacting the device electrodes (such as the source, drain, gate, and the like) through vias in an interlevel dielectric.

With the above resolution of the indefiniteness issues, all claims are now believed to be in condition for Allowance, and allowance is so requested.

The Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

It is requested that should there be any problems with this Amendment, please call the undersigned Attorney at (845) 452-5863.

Respectfully submitted,

Stephen B. Ackerman, Reg. No, 37,761

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Please cancel Claims 26-28

29. A semiconductor device structure comprising:

a semiconductor substrate [comprising] having semiconductor devices formed thereon;

an interconnecting metallization structure comprising lower metal lines, formed over and connected to said devices;

electrical contact points on an upper surface of said interconnecting metallization structure and connected to said interconnecting metallization structure;

a passivation layer deposited over said interconnecting metallization structure and over said electrical contact points;

openings through said passivation layer, exposing said electrical contact points; and

an upper metallization structure within said openings and over said passivation layer, comprising upper metal lines, connected to said interconnecting metallization structure , wherein said upper metal lines are substantially thicker than said lower metal lines.

88. A semiconductor device structure comprising:

a semiconductor substrate [comprising] having semiconductor devices formed thereon;

an interconnecting metallization structure comprising lower metal lines, formed over and connected to said devices;

electrical contact points on an upper surface of said interconnecting metallization structure and connected to said interconnecting metallization structure;

a passivation layer deposited over said interconnecting metallization structure and over said electrical contact points;

openings through said passivation layer, exposing said electrical contact points;

and

an upper metallization structure within said openings and over said passivation layer, comprising upper metal lines, connected to said interconnecting metallization structure, wherein said upper metal lines are substantially wider than said lower metal lines.

89. A semiconductor device structure comprising:

a semiconductor substrate [comprising] having semiconductor devices formed thereon;

an interconnecting metallization structure comprising lower metal lines in layers, separated by inorganic intermetal dielectric layers, formed over and connected to said devices;

electrical contact points on an upper surface of said interconnecting metallization structure and connected to said interconnecting metallization structure;

a passivation layer deposited over said interconnecting metallization structure and over said electrical contact points;

openings through said passivation layer, exposing said electrical contact points; and

an upper metallization structure within said openings and over said passivation layer, comprising upper metal lines, separated by organic dielectric layers, connected to said

interconnecting metallization structure, wherein said organic dielectric layers are thicker than said inorganic intermetal dielectric layers.

Please cancel non-elected claims 90-99.